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EXAMINER
HOGANS, DAVID L

ART UNIT	PAPER NUMBER
2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/941,817	Applicant(s) SEIBEL ET AL.	
	Examiner David L. Hogans	Art Unit 2813	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 6, 8-11, 15, 18 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over 5,966,605 to Ishida in view of 6,365,476 to Talwar et al.

Claims 1 and 11

Ishida teaches a polysilicon gate structure (56) overlying an insulation layer (54), which overlies a silicon substrate (50). Ishida also teaches doping the polysilicon gate structure (Figure 2b) and annealing the doped gate structure with a laser (Figure 2c) to promote crystallization and distribution of the dopant. (See column 3 lines 16-60 and Figures 2a-2c) Furthermore, Ishida teaches an alternative embodiment where the dopant layer (100) is formed on top of the polysilicon gate structure (56). (See column 4 lines 25-35 and Figure 2e)

Ishida fails to explicitly teach an amorphous silicon layer on top of and in contact with the insulation layer.

However, Talwar et al., in column 4 lines 14-16, teaches a gate layer (112) made from amorphous silicon laid over top of an insulation layer (114). Further, Talwar et al. teaches that laser radiation can be controlled to amorphous silicon regions because the melt temperature of crystalline silicon is about 250 °C higher than amorphous silicon. (See column 6 lines 24-27) This allows selective melting of amorphous regions thereby allowing diffusion of dopants in this region with an abrupt junction noted at the liquid-solid interface because the diffusivity of dopants in solid silicon is eight orders of magnitude lower than that of molten silicon. (See column 6 lines 30-35)

It would have been obvious to one of ordinary skill in the art to modify Ishida's teachings in view of Talwar's et al. teachings of a gate layer (112) made from amorphous silicon laid over top of an insulation layer (114). Ishida's modification via Talwar's et al. teachings is obvious because laser irradiated amorphous silicon promotes dopant diffusion due to its molten state, whereas crystalline silicon is solid and exhibits low dopant diffusivity.

Claim 2

Incorporating all arguments of Claim 1 above and noting that Ishida teaches doping the polysilicon gate (56) by ion implantation. (See column 3 lines 35-40 and Figure 2b)

Claims 3 and 15

Incorporating all arguments of Claims 1 and 11 above and noting that Ishida teaches a radiation beam that is a laser beam. (See column 3 lines 45-51 and Figure 2c)

Claims 6 and 18

Incorporating all arguments of Claims 1 and 11 above and noting that Ishida teaches depositing remaining layers such as a gate contact. (See column 4 lines 18-22)

Claims 8 and 20

Incorporating all arguments of Claims 1 and 11 above and noting that Ishida teaches an insulation layer (54) made from silicon dioxide. (See column 3 lines 25-27 and Figure 2a)

Claims 9 and 21

Incorporating all arguments of Claims 1 and 11 from above, and noting that Ishida fails to explicitly teach a dopant from at least one of boron, BF_2, indium, arsenic, phosphorus and antimony.

However, Talwar et al., in column 4 lines 45-48, teaches doping silicon with boron, phosphorus, arsenic or antimony. Examiner notes that it is well known and conventional in the art to negatively and positively dope silicon and germanium with

boron, phosphorus, arsenic or antimony. (See Microchip Fabrication, Peter Van Zant, Fourth Edition, McGraw-Hill Publishing, page 331, 2000)

It would have been obvious to one of ordinary skill in the art to modify Ishida's teachings in view of Talwar's et al. teachings of doping silicon with boron, phosphorus, arsenic or antimony. Ishida's modification via Talwar's et al. teachings is obvious because, it is well known and conventional in the art to negatively and positively dope silicon and germanium with boron, phosphorus, arsenic or antimony.

Claims 10 and 22

Incorporating all arguments of Claims 1 and 11 from above, and noting that Ishida fails to explicitly teach a gate height of less than 500 nanometers.

However, Talwar et al., in column 3 lines 56-59, teaches a gate height of 200 nanometers. Examiner notes that it is well known and conventional in the art to reduce transistor dimensions to increase device speed. Furthermore, Talwar's et al. functional use of a 200 nanometer gate renders its application obvious.

It would have been obvious to one of ordinary skill in the art to modify Ishida's teachings in view of Talwar's et al. teachings of a gate height of 200 nanometers. Ishida's modification via Talwar's et al. teachings is obvious because, it is well known and conventional in the art to reduce transistor dimensions to increase device speed.

Furthermore, Talwar's et al. functional use of a 200 nanometer gate renders its application obvious.

3. Claims 4, 5, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over 5,966,605 to Ishida in view of 6,274,488 to Talwar et al.

Claims 4, 5, 16 and 17

Incorporating all arguments of Claims 1, 3, 11 and 15 and noting that Ishida fails to explicitly teach a pulsed laser having a wavelength of between 0.1 and 2.0 microns, a temporal pulse width of less than 1 ms, and an irradiance between 0.1 and 1000 J/cm2 per pulse. Furthermore, Talwar et al. fails to explicitly teach the above laser conditions applied between 3 and 10 pulses at a repetition rate of 200 to 400 Hz.

However, Talwar et al., in column 6 lines 12-27, teaches a pulsed laser with a wavelength between 1-2 microns, a temporal pulse width between 1 to 100 nanoseconds, an irradiance between 0.1 and 10 J/cm2, at 3 to 10 pulses and a repetition rate of 200 to 400 Hz. Furthermore, Talwar et al. teaches that the above laser parameters are dependent upon the laser used and the materials affected by the laser. Therefore, the desired results (amorphous silicon crystallization and dopant diffusion) are due to obvious experimentation.

It would have been obvious to one of ordinary skill in the art to modify Ishida's teachings in view of Talwar's et al. teachings of a pulsed laser with a wavelength between 1-2 microns, a temporal pulse width between 1 to 100 nanoseconds, an irradiance between 0.1 and 10 J/cm2, at 3 to 10 pulses and a repetition rate of 200 to 400 Hz. Ishida's modification via Talwar's et al. teachings is obvious because the desired results (amorphous silicon crystallization and dopant diffusion) are due to obvious experimentation. Furthermore, Talwar's et al. functional use of the above laser parameters renders its application obvious.

4. Claims 7, 12-14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over 5,966,605 to Ishida.

Claims 7 and 19

Incorporating all arguments of Claims 1, 6, 11 and 18 and noting that Ishida fails to explicitly teach a metal contact comprised of at least one of tungsten, tungsten silicide, tungsten nitride, tantalum, tantalum nitride, titanium, titanium nitride and platinum.

However, Examiner notes that refractory metals (titanium, tungsten and tantalum) and their silicides offer a lowered contact resistance. Examiner further notes that modern circuit design, especially MOS circuits, employ refractory metals or their silicides as conductive layers due to their lower resistivity and lower contact resistance.

(See Microchip Fabrication, Peter Van Zant, Fourth Edition, McGraw-Hill Publishing, pages 403-404, 2000)

Therefore, it would have been obvious to one of ordinary skill in the art to modify Ishida because modern circuit design employs metal contacts comprised of at least one of tungsten, tungsten silicide, tungsten nitride, tantalum, tantalum nitride, titanium, titanium nitride and platinum.

Claims 12-14

Incorporating all arguments of Claim 11 and noting that Ishida teaches a dopant layer formed by chemical vapor deposition. (See column 4 lines 25-35) Examiner further notes that Ishida fails to explicitly teach a dopant layer formed by sputtering or evaporation.

However, Examiner notes that sputtering and evaporation are known and conventional within the art for vacuum deposited materials. (See Microchip Fabrication, Peter Van Zant, Fourth Edition, McGraw-Hill Publishing, page 411, 2000) Furthermore, sputtering offers the advantage of deposition of the dopant without chemical or compositional change of the dopant and evaporation deposits low energy atoms without damage to the surface substrate.

Therefore, it would have been obvious to one of ordinary skill in the art to modify Ishida because sputtering and evaporation are known and conventional within the art for vacuum deposited materials.

5. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,966,605 to Ishida in view of 6,077,758 to Zhang et al.

Incorporating all arguments of Claim 11 above and noting that Ishida fails to explicitly teach dopant concentrations of at least one of boron, arsenic and phosphorus up to $3x10^{20}$ ions/cm^3, $5x10^{20}$ ions/cm^3, and $1x10^{21}$ ions/cm^3, respectively.

However, Zhang et al., in column 10 lines 51-55, teaches a doping concentration of phosphorus or boron between 10^{19} and 10^{21} cm^{-3}. Examiner notes that it is known and conventional within the art to dope silicon with boron or phosphorus at concentration levels of 10^{19} to 10^{21} ions/cm^{-3}, to reduce or lower resistivity.

It would have been obvious to one of ordinary skill in the art to modify Ishida's teachings in view of Zhang's et al. teachings of a doping concentration of phosphorus or boron between 10^{19} and 10^{21} cm^{-3}. Ishida's modification via Zhang's et al. teachings is obvious because it is known and conventional within the art to dope silicon with boron or phosphorus at concentration levels of 10^{19} to 10^{21} ions/cm^{-3}, to reduce or lower

resistivity. Furthermore, Zhang's et al. functional use of the above doping concentrations, renders its application obvious.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Hogans whose telephone number is (703) 305-3361. The examiner can normally be reached on M-F (7:30-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Doug Wille
Patent Examiner

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April 15, 2002